

REMARKS

Claims 1-7, 23 and 25-34 are currently pending in the subject application and are presently under consideration. Claims 1, 7, and 34 have been amended as shown on pages 2-4 of the Reply.

Favorable reconsideration of the subject patent application is respectfully requested in view of the comments and amendments herein.

I. Rejection of Claims 1-7, 23, 25-26 and 32-34 Under 35 U.S.C. §103(a)

Claims 1-7, 23, 25-26 and 32-34 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Dhindsa, *et al.* (U.S. 5,740,016). Withdrawal of this rejection is requested in view of at least the following. Dhindsa, *et al.* does not teach or suggest all aspects recited in the subject claims.

The claimed subject matter generally relates to regulating heat in an integrated circuit device, and in particular to removing generated heat from hot spot areas. To this end independent claims 1, 7 and 34 recite similar features namely: ***at least one of the plurality of the thermoelectric structures has a distribution of line patterns that is denser towards center of its structure and decreases in density towards outer limits of the structure wherein the at least one thermoelectric structure is coupled to an associated hot spot.*** The cited art does not teach or suggest such claimed aspects.

Dhindsa, *et al.* relates to a solid state temperature controlled substrate support for maintaining a desired temperature distribution across a substrate during processing in semiconductor equipment. Accordingly, it teaches a temperature controlled substrate support included in a semiconductor processing system for processing a substrate. A substrate resting on the substrate support surface is inserted into a processing chamber and processed to produce integrated chips. The substrate support includes a plurality of thermoelectric modules and by controlling the current supply to each of these modules to provide temperature uniformity across the substrate during processing (*See Dhindsa, et al.* col.2 lines 35-55). Thus, Dhindsa, *et al.* relates to maintaining temperature uniformity during production of integrated chips as the substrate support surface bearing the thermo-electric modules is used in the processing chamber. However, it does not teach or suggest including the thermoelectric structures into the integrated circuit in order to prevent formation of hot-spots as recited in the subject claims. Moreover, as

conceded on page 3 of the subject Office Action Dhindsa, *et al.* does not teach or suggest a specific structure for each thermoelectric structure. A broad assertion that a plurality of thermoelectric modules can be arranged in any particular manner cannot teach a specific form for an individual thermoelectric structure as recited in the subject claims.

Although no formal rejection is made, the Examiner attempts to overcome these deficiencies of Dhindsa, *et al.* by citing various other documents. On page 4 of the subject Office Action it is erroneously contented that Macris (U.S.6727422) discloses a thermoelectric structure with line patterns that are denser at the center and less dense at the outer edges. Applicants' representative respectfully disagrees. At the cited portion, there are no lines at the center. This is more clearly seen in Fig.9A of Macris, which shows a single thermo-element couple. (See Fig.9A and col.6 lines 18-19 of Macris). Similarly, another document Bell (U.S.7231772) relates to non-analogous art of solid-state cooling, heating and power generation system (See Bell col.1 lines 15-17). On page 4 it is erroneously contented that Bell discloses a thermoelectric structure with denser distribution of lines at the center and less dense distribution at the periphery. However, at the cited portion in Fig.7D, there are no lines at the center, only moving media 708. Similarly, in another document Saika (U.S.6573596) Figs. 3-6 disclose different arrangements for a plurality of Peltier devices in a thermo module, but it does not teach or suggest an arrangement for an individual Peltier device.

In contrast to these documents, the subject claims relate to a thermoelectric structure couple with an associate hot spot with a pattern made up of denser distribution of lines at the center and less dense line patterns at the outer edges of the structure. These line patterns are better able to address localized heating problems within semiconductor integrated circuits since when coupled with hot spots, the denser line patterns can absorb heat faster. None of the cited documents teach nor suggest such novel aspects.

In view of at least the foregoing, it is respectfully requested that this rejection be withdrawn with respect to independent claims, 1, 7, 34 as well as all claims that depend there from.

II. Rejection of Claim 27 Under 35 U.S.C. §103(a)

Claim 27 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Dhindsa, *et al.* (U.S. 5,740,016) in view of Ghoshal (U.S. 6,105,381). Withdrawal of this rejection is requested for at least the following reasons. As stated *supra*, Dhindsa, *et al.* fails to teach or suggest all aspects of the independent claim 1 from which claim 27 depends and Ghoshal fails to make up for this deficiency. In particular, Ghoshal fails to teach or suggest a thermoelectric structure with line patterns as recited in independent claim 1. Hence, this rejection should be withdrawn with respect to claim 27 which depends there from.

CONCLUSION

The present application is believed to be in condition for allowance in view of the above comments and amendments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [AMDP812US].

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number below.

Respectfully submitted,

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